WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device including a clock synchronous type circuit that operates in synchronization with one of a rising edge flank and a falling edge flank of a reference clock and a plurality of clock buffer circuits for distributing a reference clock to said clock synchronous circuit, wherein

each of said clock buffer circuits comprises an inverter including:

a first transistor for driving a load at one of edges flank of the reference clock with which said clock synchronous circuit does not operate in synchronization; and

a second transistor for driving the load at the other edge flank of the reference clock with which said clock synchronous circuit operates in synchronization, a type of carriers used in a channel for the second transistor being different from the carrier type of the first transistor and the second transistor being formed to have a gate width larger than the first transistor.

2. The semiconductor integrated circuit device according to claim 1, wherein the first transistor is a P-channel field-effect transistor;

the second transistor is an N-channel field-effect transistor; and

said clock synchronous circuit operates in synchronization with the falling edge flank of the reference clock.

3. The semiconductor integrated circuit device according to claim 1, wherein said first transistor has a gate width of the first transistor being set so that a change in the edge flank is slowed down provided that a pulse waveform of the reference clock is not destroyed.

4. The semiconductor integrated circuit device according to claim 1, comprising:

a first-stage inverter displaced in an input stage of said each of said clock buffer circuits, the first-stage inverter comprising:

an N-channel field-effect transistor having a gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having a gate width larger than the N-channel field-effect transistor.

5. The semiconductor integrated circuit device according to claim 2, comprising:

a first-stage inverter displaced in an input stage of said each of said clock buffer circuits, the first-stage inverter comprising:

an N-channel field-effect transistor having a gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having a gate width larger than the N-channel field-effect transistor.

6. The semiconductor integrated circuit device according to claim 1, comprising:

a gate circuit displaced in an input stage of said each of said clock buffer circuits, for supplying the reference clock to the inverter according to an enable signal, the gate circuit comprising:

an N-channel field-effect transistor having the gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having the gate width larger than the N-channel field-effect transistor.

7. The semiconductor integrated circuit device according to claim 2, comprising:

a gate circuit displaced in an input stage of said each of said clock buffer circuits, for supplying the reference clock to the inverter according to an enable signal, the gate circuit comprising:

an N-channel field-effect transistor having the gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having the gate width larger than the N-channel field-effect transistor.

8. The semiconductor integrated circuit device according to claim 6, wherein the gate circuit is a NAND gate.

9. The semiconductor integrated circuit device according to claim 1, having a clock tree synthesis configuration made up using said clock buffer circuits.